What is Claimed is:

[c1] A semiconductor comprising:
a contact having a portion that extends on two opposing vertical sides of at least one vertical structure adjacent a gate electrode.

[c2] The semiconductor of claim 1, wherein the contact contacts a substrate adjacent the at least one spacer.

[c3] The semiconductor of claim 1, wherein the contact contacts the gate electrode.

[c4] The semiconductor of claim 1, wherein the contact includes an upper portion that is larger than a lower, contact portion.

[c5] A method of forming a contact, comprising the steps of:
defining a vertical structure on a substrate;
depositing a first layer over the substrate;
selectively removing the first layer to form an opening having two edges spaced from one another, the opening exposing the vertical structure, at least one of the edges of the opening being disposed a distance from the vertical structure to define a masking space;
depositing a second layer across the opening including the masking space;
selectively removing the second layer outside the masking space while retaining at least a portion of the second layer within the masking space; and
depositing a conductor within the opening and on a remaining portion of the second layer.

[c6] The method of claim 5, wherein the first layer is a dielectric and the second layer is a conformal layer.

[c7] The method of claim 5, wherein the step of removing includes isotropically etching.

[c8] The method of claim 5, wherein the distance is sized to allow filling of the masking space with the second layer.

[c9] The method of claim 5, wherein the masking space is over a gate electrode and the conductor contacts the substrate.

[c10] The method of claim 5, wherein the masking space is in contact with the substrate and the conductor contacts a gate electrode.

[c11] The method of claim 5, wherein the vertical structure is at least one spacer of a gate electrode, the at least one spacer extending vertically beyond the gate electrode.

[c12] The method of claim 11, wherein the conductor extends on two sides of the at least one spacer.

[c13] The method of claim 11, further comprising the step of forming silicide in at least one of the gate electrode and adjacent diffusion areas prior to the step of depositing the first layer.

[c14] A method of depositing a material in a first space of an opening without depositing the material in a second space of the opening, the opening and the first and second space being on or above a substrate, the second space having at least one lateral dimension that is smaller than the first space, the method comprising the steps of:
forming a vertical structure on the substrate, the vertical structure being disposed in the opening to define the first and second space;
depositing a layer so that the layer fills the second space and covers the first space;
selectively removing the layer in the first space while retaining at least a portion of the layer in the second space; and
depositing the material.

[c15] The method of claim 14, wherein the vertical structure is a spacer of a gate electrode, the spacer extending above an upper surface of the gate electrode.

[c16] The method of claim 15, wherein the vertical structure is a pair of spacers of the gate electrode, each spacer extending above an upper surface of the gate electrode.

[c17] The method of claim 16, wherein the material extends on two vertical sides of each spacer.

[c18] The method of claim 14, wherein the material is a conductor.

[c19] The method of claim 14, wherein the second space is over a gate electrode and the material contacts the substrate.

[c20] The method of claim 14, wherein the second space is in contact with the substrate and the material contacts a gate electrode.